MARKED COPY OF SPECIFICATION PARAGRAPHS

SERIAL NO. 09/712,105

DOCKET: NEC 00USFP553

MARKED SPECIFICATION PARAGRAPHS SHOWING CHANGES MADE

Paragraph beginning at page 1, line 13:

In recent semiconductor devices, new [form] forms of packages have been developed to comply with demands for electronic devices having high performance, small size, light weight, and high speed. Smaller and slimmer devices have been realized by high integration of semiconductor chips to be mounted, and much higher performance and speed are aimed at electronic devices. A package according to FCBGA (Flip Chip Ball Grid Array) method has appeared.

Paragraph bridging pages 3-4, beginning at line 26:

A package according to the FCBGA method is generally used for a large-scale semiconductor integrated circuit (LSI) having high performance, and the product itself is expensive. Therefore, if an error is detected in other parts than the semiconductor chip through an electrical selection process after actual installation of the semiconductor chip, the semiconductor chip is detached from the multi-layer printed circuit board and is used again. In the process of the detachment, as shown in Fig. 1C, the non-defective semiconductor chip 31 is heated and suctioned and pulled up by a suction heat tool 33, while the bump connecting sections is [melt] melted. Thus, the non-defective semiconductor chip 31 is detached from the multi-layer printed circuit board 32.

Paragraph beginning at page 5, line 2:

In conjunction with the above description, a [ship] chip size package is disclosed in Japanese Laid Open Patent Application (JP-A-Heisei 9-64236). In this reference, a chip 10 is connected to a laminate circuit board 20 via direct through-noles 30 in a flip-chip manner. The laminate circuit board 20 has the same size as the chip 10. A gap between the laminate circuit

board 20 and the chip 10 is filled with under-fill (40). The chip 10 is connected to external terminals 50 via wiring lines 21 to 24 and via-holes 31. The whole chip 10 including the board 20 is covered other than openings 61 by encapsulant.

Paragraph bridging pages 6-7, beginning at line 22:

Also, a test connector is disclosed in Japanese Patent No. 2,658,831. In this reference, the test connector is produced through an electrode section opening process, an electrode embedding process and an electrode finishing process. A test semiconductor device to be tested has bumps on its surface. The bumps are connected by a flip chip method in which wiring lines are not used. The test connector has a sheet-like shape and electrodes supported by a supporting substrate are connected to the bumps for an electric test. In the electrode opening process, openings for electrode sections are formed in a sheet using a punch and a die. in the electrode section embedding process, electrodes are inserted in the openings and then heat-resistant insulating material is injected and hardened as an insulting film. In the electrode section [fining] finishing process, the sheet is removed. Thus, ends of each of the electrodes protrude from the insulating film.

Paragraph bridging pages 7-8, beginning at line 26:

Still another object of the present invention is to provide a semiconductor device, in which [damages] damage during recovery process for peripheral devices including an installation board can be avoided to realize low costs.

Paragraph beginning at page 8, line 4:

In order to achieve an aspect of the present invention, a semiconductor device includes pads formed on a semiconductor chip, conductive sections connected to the pads, respectively, conductive bumps on surfaces of the conductive sections, and an insulating film covering the

semiconductor chip other than the surfaces of the conductive sections. The insulating film [including] includes a stress buffering layer in a lateral direction of the conductive sections to relax a stress applied to the bumps.

Paragraph beginning at page 9, line 10:

Also, the insulating film may comprise a first and a second insulating film and the conductive section may be connected to the pad via a wiring pattern provided on the semiconductor chip [via a] through the first [insulting] insulating film [of the insulating film]. In this case, it is desirable that the wiring pattern is formed of copper (Cu). Also, the wiring pattern may extend to adjust a pitch between the conductive bump and another conductive bump. Further, the first insulating film may include a passivation film covering the semiconductor chip other than the pads, and a second insulating film formed on the passivation film. In this case, it is desirable that the second insulating film has a pyrolysis temperature of 200° C or more. in addition, the second insulating film may be formed of a photosensitive material.

Paragraph beginning at page 14, line 4:

Next, as [sown] shown in Fig. 2B, an insulative resin film (insulating layer) 20 is formed on the pad electrodes 12 and a passivation film 13. The insulating resin film 20 is made of inorganic material such as SiO_2, or organic material such as polyimide (PI). Resin material having a pyrolysis temperature of 200° C or more is used for the insulating resin film 20. When material of a thermal hardening component is mixed in the insulating resin film 20, heat treatment is carried out at a predetermined temperature thereby to promote bridging reaction of resin components. Thus, predetermined physical and chemical properties are attained.